CSMSS's

Chh. Shahu College of Engineering,

Kanchanwadi, Chh. Sambhaji Nagar

Affiliated to

Dr. Babasaheb Ambedkar Technological University

Lab Manual

of

ANALOG AND DIGITAL ELECTRONICS LAB (BTEEL409)

for

BTech EE Semester IV

Department of Electrical Engineering

CSMSS
Chhatrapati Shahu Maharaj Shikshan Sanstha's
CHH. SHAHU COLLEGE OF ENGINEERING
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Approved by AICTE New Delhi, DTE (Govt. of Maharashtra) and affiliated to Dr. BATU, Lonere (Raigad). DTE Code: 2533

Vision and Mission of the Institute

Vision:

To be an institution of repute through multidisciplinary educational approach to develop the next generation competent technocrats for industry and society.

Mission:

M1:	Developing student centric educational practices for curriculum delivery and assessment.
M2:	Imparting entrepreneurial and employability skills among students through value-based and skill-based training in collaboration with industry and academia.
M3:	Inculcating social and professional values among students through awareness and outreach activities.
M4:	Providing an environment for innovation and research through various interdisciplinary activities.

CSMSS CHH. SHAHU COLLEGE OF ENGINEERING * DTE CODE 2533 * AURANGABAD *

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CSMSS
CHH. SHAHU COLLEGE OF ENGINEERING
KANCHANWADI, AURANGABAD - 431002

VISION AND MISSION OF DEPARTMENT

Vision

To be a role model in developing electrical engineering graduate with knowledge, skill & ethics.

Mission

We, at department of electrical Engineering, are committed to achieve our vision by-
M1-quality education, training, knowledge and skill necessary to excel in their careers.
M2-research and development, innovative solution that are efficient, sustainable and responsive to the needs of industry and society.
M3-diversity, equity and inclusion in all aspects of department's activities, supportive and inclusive environment
M4-resources for local community, providing expertise, advice and solution related to electrical engineering

PROF.A.N.MUDIRAJ
HEAD OF DEPARTMENT

Class: BTech Electrical Engineering

Subject: ANALOG AND DIGITAL ELECTRONICS LAB (BTEEL409)

Teaching Scheme
Practical: 02 hrs/week

Exam Scheme
Practical: 40 marks

List of Practical's

Practical No	Title
1	To Study Op-Amp as an Integrator.
2	To Study Op-Amp as Differentiator.
3	Verify the operation of voltage comparator circuit and zero crossing detector circuit using Op-Amp 741 IC.
4	To study Schmitt trigger circuit using Op-Amp IC 741.
5	To study working of Instrumentation amplifier circuit using IC 741.
6	To study basic Logic Gates and verify truth table such as AND OR NOT
7	To Study Multiplexer operation Using IC-74150.
8	To Study De-Multiplexer operation Using IC-74138.
9	To study operation of Fip-Flops SE, D- FF and JK- FF.

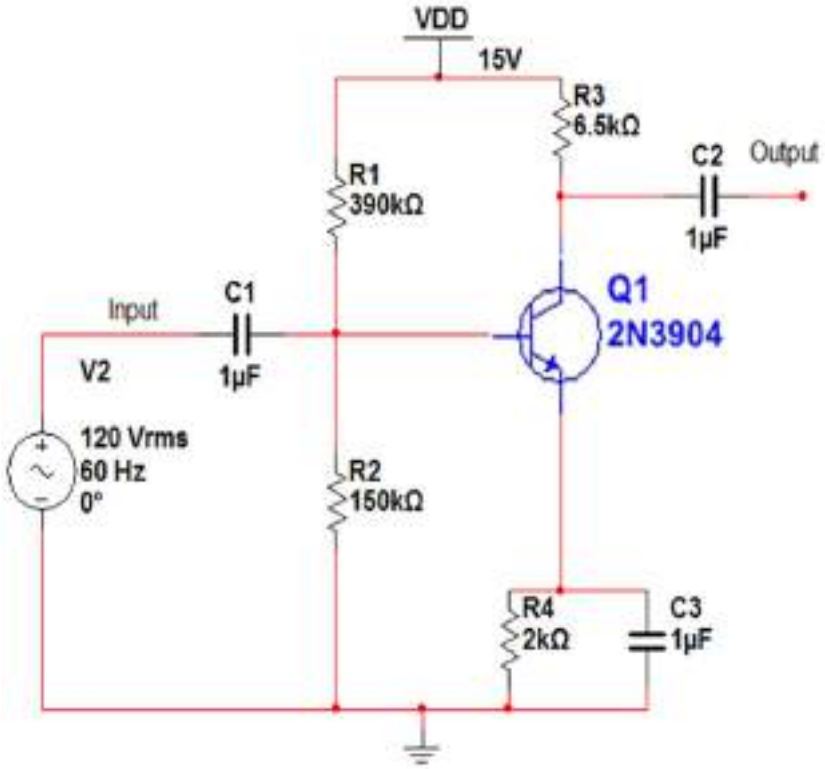
Experiment No.

Experiment no 1

Aim: To study Frequency Response of single stage BJT Amplifier

Equipments: Transistor 2N3904, DC supply, function generator, CRO, two capacitors, 4 resistors

Circuit diagram:



Theory:

Amplifier is an electronic circuit that is used to raise the strength of a weak signal. The process of raising the strength of a weak signal is known as amplification. One importance requirement during amplification is that only the magnitude of the signal should increase and there should be no change in signal shape. The transistor is used for amplification. When a transistor is used as an amplifier, the first step is to choose a proper configuration in which device is to be used. Then the transistor is biased to get the desired Q-point. The signal is applied to the amplifier input and gain is achieved.

Procedure :

1. Feed 100mV (peak-to-peak) sinusoidal signal at 1 KHz frequency as the input signal Vs to the CE circuit.

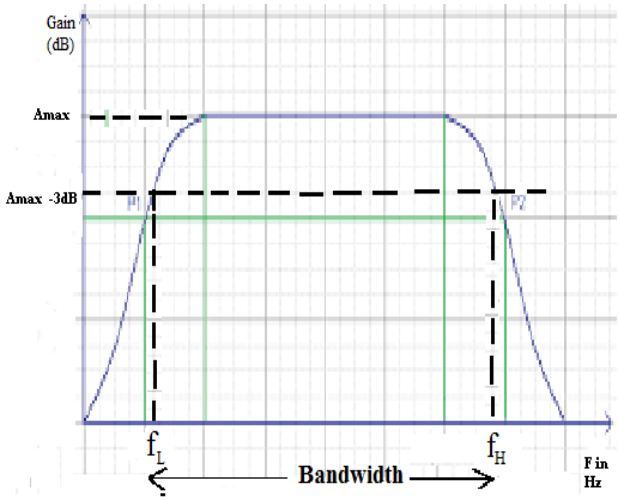
2. Now increase the frequency from 1 KHz to 1MHz and measure the voltage gain of the amplifier at each frequency.

3. Take at least 5 readings on either side of the 1 KHz frequency. Tabulate the reading.
4. Plot on a semi log graph sheet the frequency response (voltage gain vs frequency) curve using the above measurements.
5. From the plot, determine the values of (a) Mid band voltage gain, AV(mid), (b) Lower cut-off frequency, (c) Upper cut-off frequency and (d) Bandwidth. Input Voltage, VS = _____ mV.

Observation table :

Signal frequency(Hz)	**Output Voltage (Volts)**	**Gain in dB**

Result:



Experiment no 2

Aim: - Measurement of op-amp parameters viz. Input offset voltage, Bias current, Slew rate and CMRR.

Apparatus: - IC 741, Resistors, Function generator, CRO, CRO probes, Dual power supply.

Circuit diagram:-

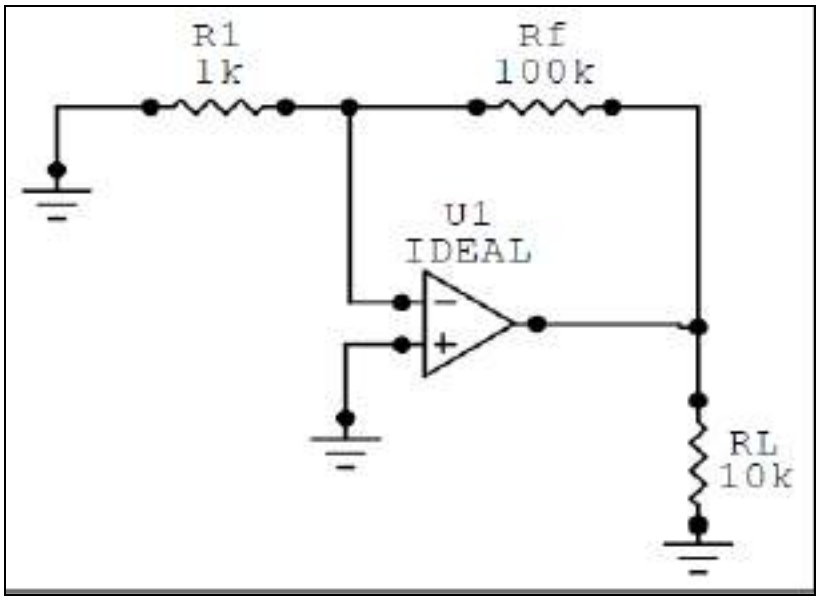


Fig 1: Input offset voltage

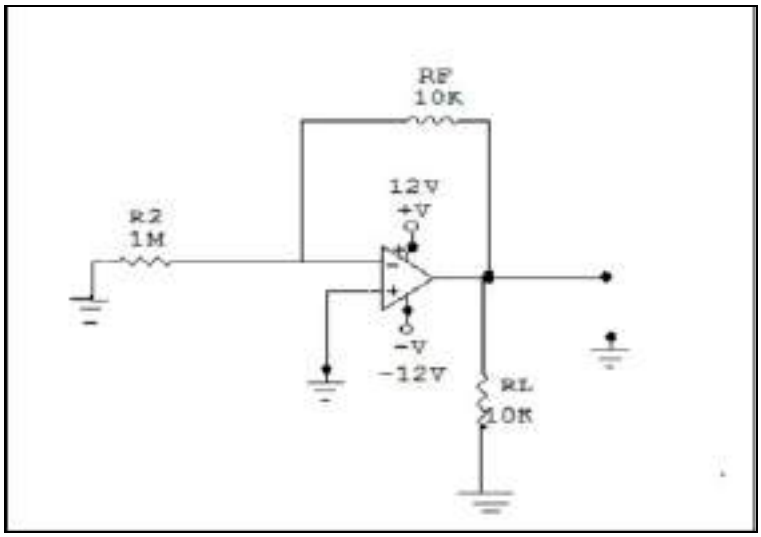


Fig 2: Bias current

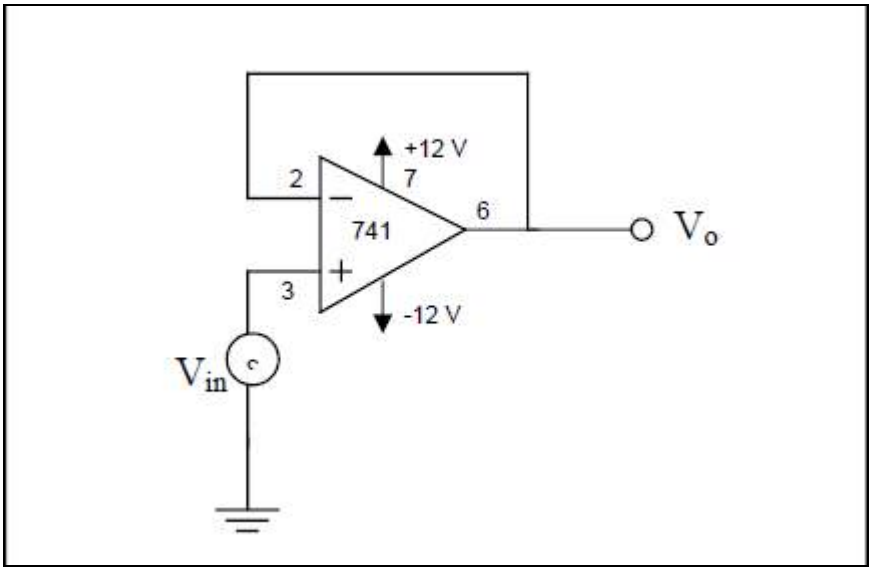


Fig.3 Measurement of Slew rate

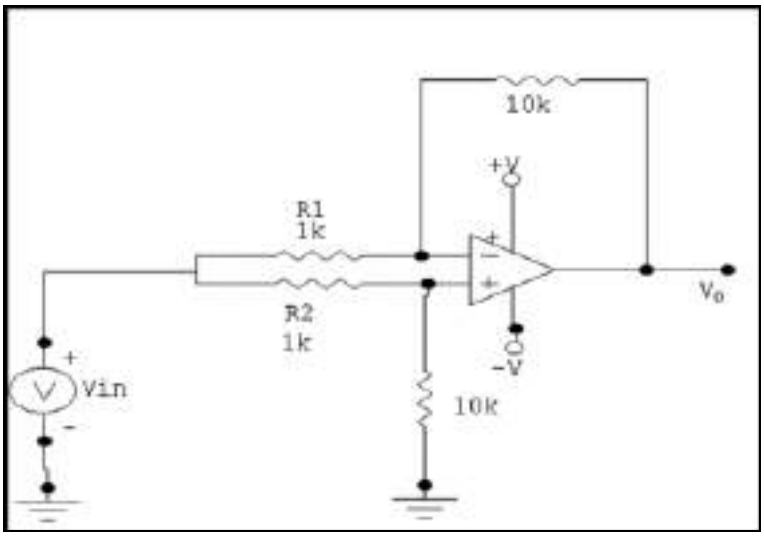


Fig 4: Common Mode for CMRR

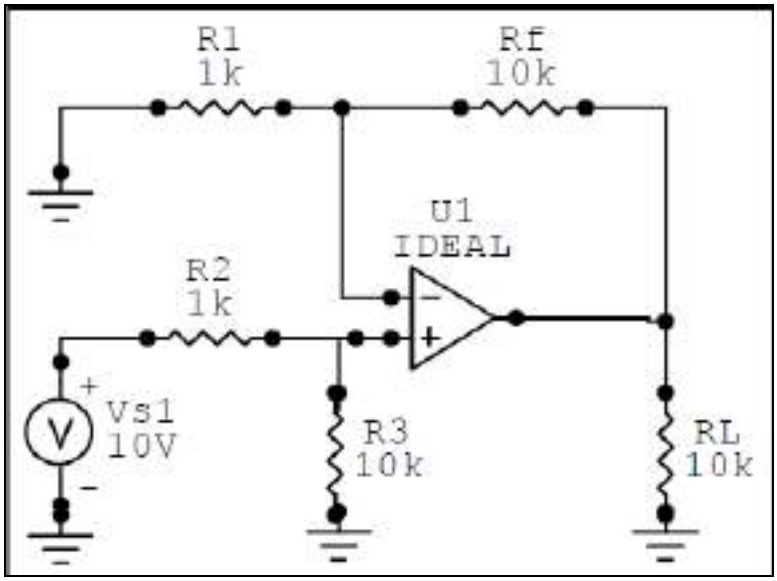


Fig 5: Differential Mode for CMRR

THEORY: - Describe all parameters of OP-AMP.

PROCEDURE: - For Input Offset Voltage
1. Make connections as shown in figure.
2. Measure the output voltage.
3. Calculate the value of input offset voltage.

For Input Bias Current
1. Make connections as shown in figure.
2. Measure the output voltage.
3. Calculate the value of input bias current by using given formula.

For Slew Rate
1. Make connections as shown in figure.
2. Note down the value of Vpeak.
3. Vary the frequency of input voltage & observe the output waveform.
4. Note the value of frequency at which output waveform start distorting.
5. Calculate the value of slew rate using given formula.

For CMRR
1. Make connections as shown in the figure.
2. Give i/p voltage of 1v peak to peak.
3. Measure the differential & common mode output.
4. Calculate Ad, Acm, & CMRR in db using formula.

***OBSERVATION:* - For Input offset voltage and Bias current**

V_{oo} (For V_{ios})	V_o (For I_b)

For Slew rate

Input frequency	Remark

For CMRR

Vo1= Vo2=

Formulae : - **For Input offset voltage**

$V_{io} = V_{oo} / (1 + R_f/R_{1)}$

For bias current

$V_o = I_B * R_F$

$I_B = V_o / R_F$

For Slew rate

$$SR = \frac{2\pi \times f_{max} \times V_p}{10^6} \quad V/\mu s$$

For CMRR

$CMRR = 20 \log(A_d/A_c)$

$Ad = V_{o1}/V_{in}$

$Acm = V_{o2}/V_{in}$

$CMRR = 20 \log(V_{o1}/V_{o2})$

RESULT:-

Sr. No.	Op Amp Parameter	Theoretical value for IC 741	Calculated Value
1	Input Offset Voltage		
2	Input Bias Current		
3	Slew Rate		
4	CMRR		

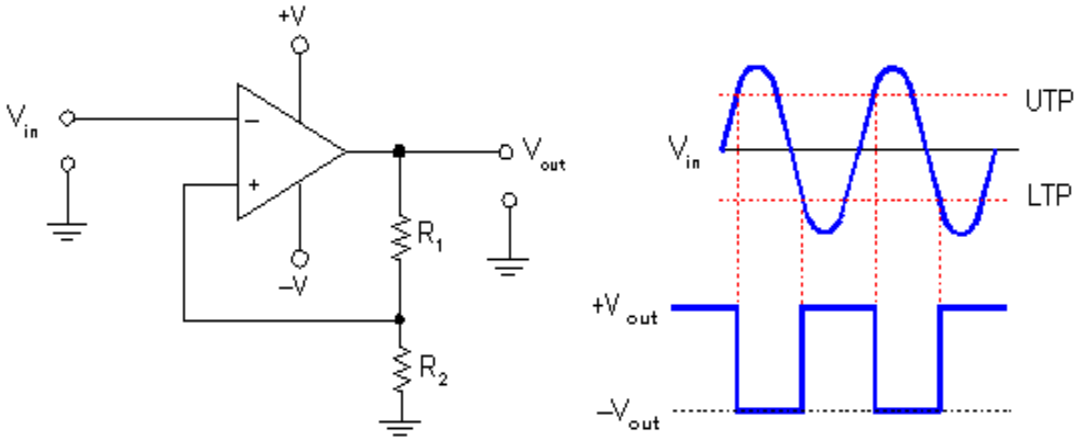
CONCLUSION:-

Experiment 3

AIM: To study Schmitt trigger using IC 741.

Apparatus: IC 741, resistors, frequency generator, CRO probes, dual power supply.

Diagram:



Theory:

Schmitt trigger circuit is implemented by an inverting comparator circuit of op-amp. In the inverting version, the attenuation and summation are separated. The two resistors R1 and R2 act only as a voltage divider. The purpose of the Schmitt trigger is to convert any regular or irregular shaped input waveform into a square wave output voltage or pulse. Thus, it can also be called a squaring circuit.

When **Vout = +Vsat,** the voltage across R1 is called **Upper Threshold Voltage (Vupt**). The input voltage, Vin must be slightly more positive than Vupt inorder to cause the output Vo to switch from +Vsat to -Vsat. When the input voltage is less than Vupt, the output voltage Vout is at +Vsat.

Upper Threshold Voltage, Vupt = +Vsat (R1/[R1+R2])

When **Vout = -Vsat**, the voltage across R1 is called **Lower Threshold Voltage (Vlpt)**. The input voltage, Vin must be slightly more negaitive than Vlpt inorder to cause the output Vo to switch from -Vsat to +Vsat. When the input voltage is less than Vlpt, the output voltage Vout is at -Vsat.

Lower Threshold Voltage, Vlpt = -Vsat (Rdiv1/[R1+R2])

Schmitt triggers are typically used in open loop configurations for noise immunity and closed loop configurations to implement function generators.

Procedure:

1) Give 14v supply to pin 7 of IC741 and -14 V to pin no.4.

2) Make connections as in figure.

3) Observe input and output waveforms.

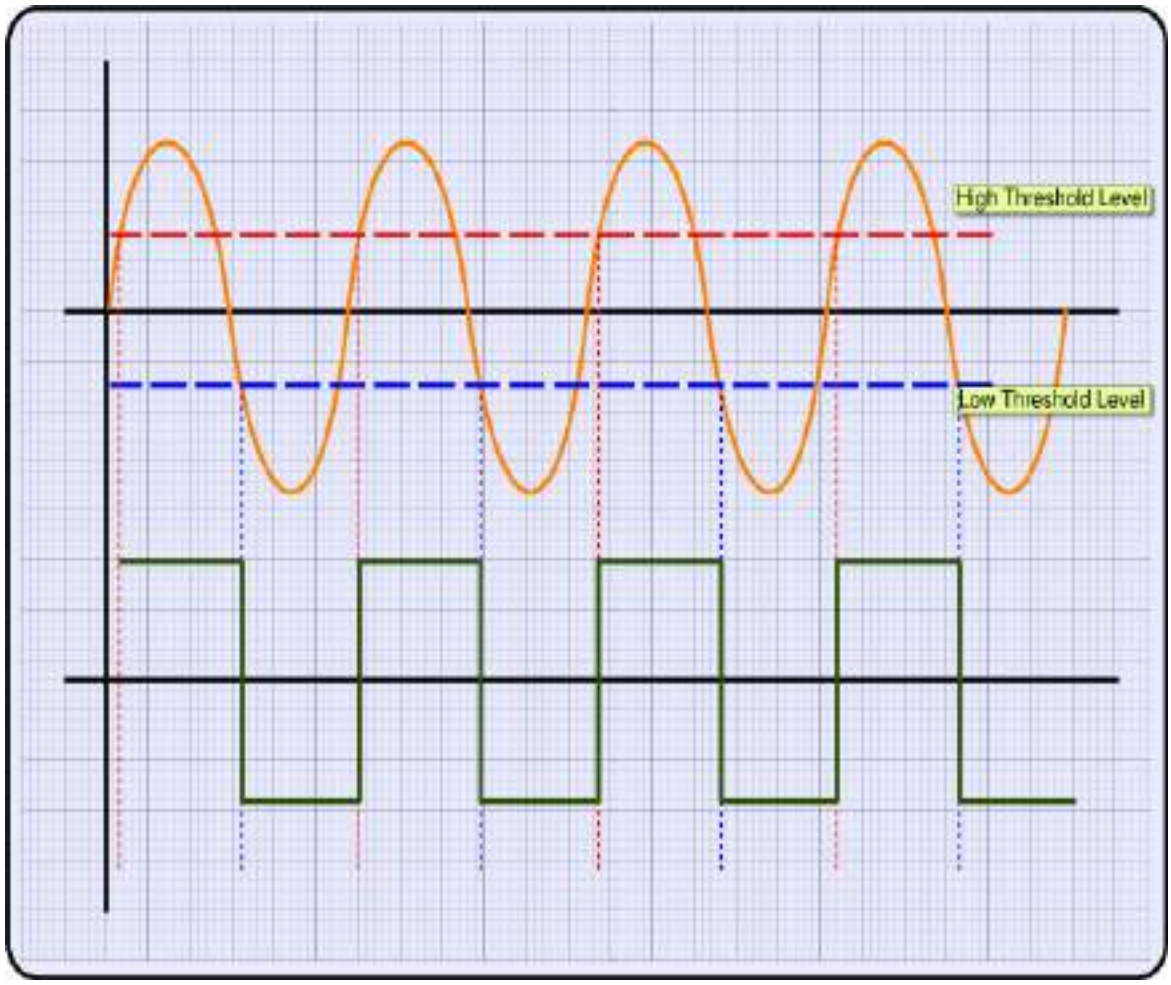
4) Plot the waveform on graph paper.

5) Draw hysteresis loop.

Calculation:

Vut: R1/(R1+R2)* (+V sat) Vlt: R1/(R1+R2)* (-V sat)

Input and Output waveforms:



Conclusion:

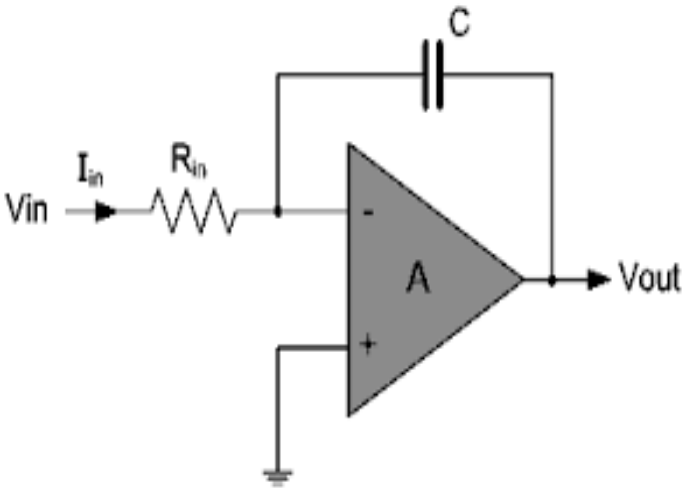
So by using op-amp we can implement Schmitt trigger which converts irregular (Here Sine wave) waveform to square wave.

Experiment No 4

I. AIM: To design and implement op-amp as an integrator and differentiator.

APPARATUS: Resistor, CRO, Frequency generator, capacitor, IC 741.

DIAGRAM:



THEORY:

By introducing electrical reactance into the feedback loops of op-amp amplifier circuits, we can cause the output to respond to changes in the input voltage over time. Drawing the name from the respective functions generated by the given op-amp circuit (***integrator)*** produces a voltage output proportional to the product (multiplication) of the input voltage and time i.e, **integration.**

PROCEDURE:

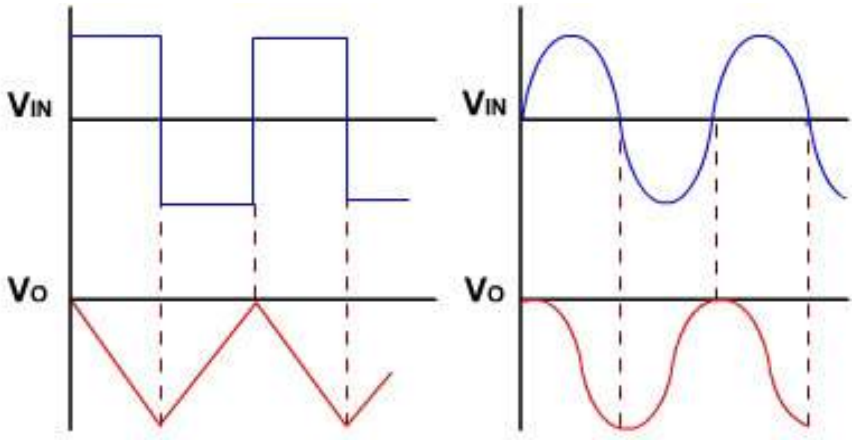
1) Give 14v supply to pin 7 of IC741 and -14 V to pin no.4.

2)Make connections as in figure.

3) Observe input and output waveforms.

4) Plot the waveform on graph pape

WAVEFORMS:

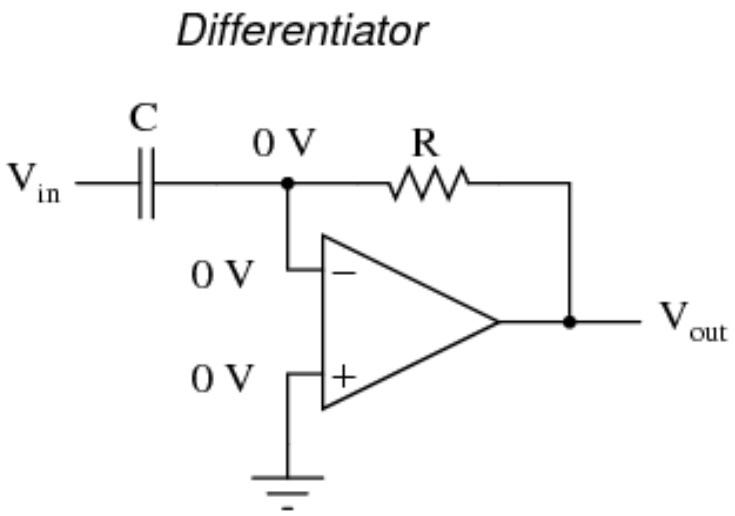


CONCLUSION: Thus an Op-amp can be used as an Integrator in different applications as ADC, Wave shaping ckts etc.

II. AIM: To study op amp as a differentiator:

APPARATUS: Resistor, CRO, Frequency generator, capacitor, IC 741.

DIAGRAM:



THEORY:

As shown in figure, the right-hand side of the capacitor is held to a voltage of **0 volts**, due to the **"virtual ground"** effect. Therefore, current "through" the capacitor is solely due to *change* in the input voltage. A steady input voltage won't cause a current through C, but a *changing* input voltage will.

Capacitor current moves through the feedback resistor, producing a drop across it, which is the same as the output voltage. A linear, positive rate of input voltage change will result in a steady negative voltage at the output of the op-amp. Conversely, a linear, negative rate of input voltage change will result in a steady positive voltage at the output of the op-amp.

This polarity inversion from input to output is due to the fact that the input signal is being sent (essentially) to the inverting input of the op-amp, so it acts like the inverting amplifier mentioned previously.

The faster the rate of voltage change at the input (either positive or negative), the greater the voltage at the output.The formula for determining voltage output for the differentiator is as follows:

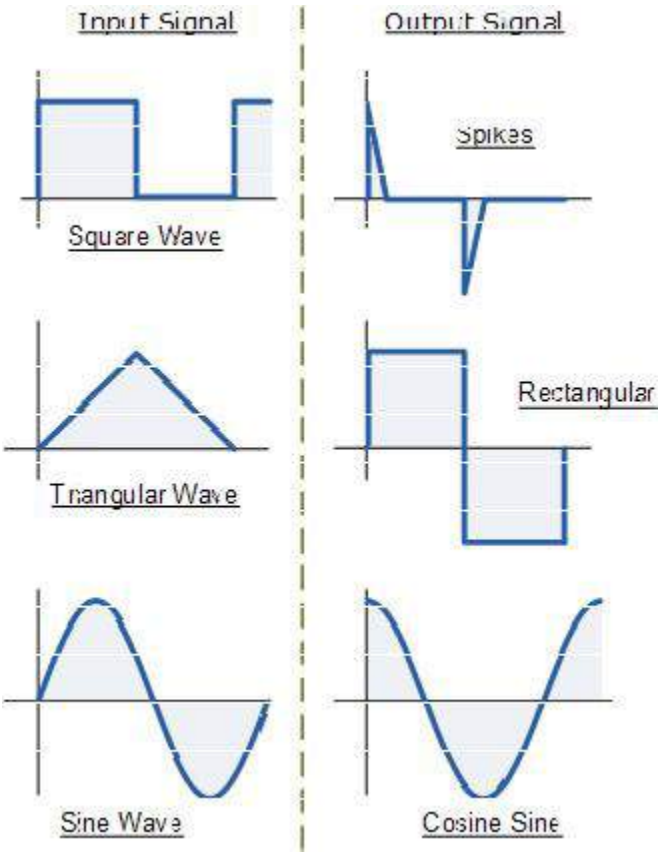
$$V_{out} = -RC \frac{dv_{in}}{dt}$$

PROCEDURE:

1) Give 14v supply to pin 7 of IC741 and -14 V to pin no.4.
2) Make connections as in figure.
3) Observe input and output waveforms.

4) Plot the waveform on graph paper.

WAVEFORMS:



CONCLUSION:

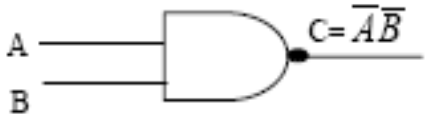
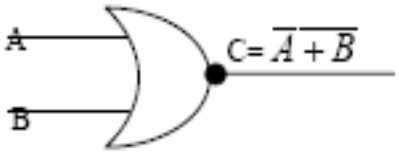
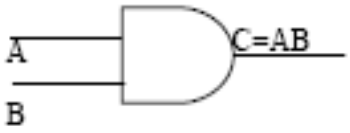
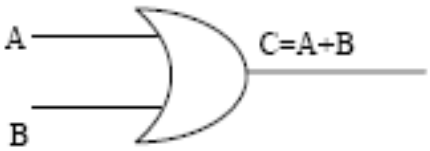
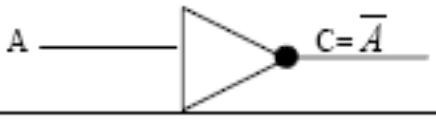
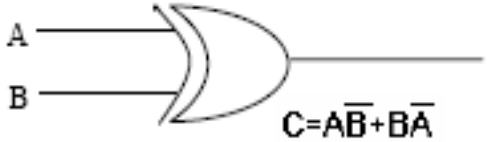
The differentiator circuit is essentially a high pass filter. It can generate a square wave from a triangle wave input, and will produce alternating-direction voltage spikes when a square wave is applied. In ideal cases, a differentiator will reverse the effects of an integrator on a waveform, and *vice versa*. Differentiators are an important part of electronic analog computers and analogue PID controllers.

Experiment 5

AIM: To learn and verify all type LOGIC GATES.

Apparatus: Logic gate trainer kit, 7404 NOT Gate, 7402 NOR Gate, 7486 XOR Gate, 7408 AND Gate ,7432 OR Gate, 7400 NAND Gate,5V adaptor, connecting wires.

Logic symbols:

S.NO	GATE	SYMBOL	INPUTS		OUTPUT
			A	B	C
1.	NAND IC 7400		0	0	1
			0	1	1
			1	0	1
			1	1	0
2.	NOR IC 7402		0	0	1
			0	1	0
			1	0	0
			1	1	0
3.	AND IC 7408		0	0	0
			0	1	0
			1	0	0
			1	1	1
4.	OR IC 7432		0	0	0
			0	1	1
			1	0	1
			1	1	1
5.	NOT IC 7404		1	-	0
			0	-	1
6.	EX-OR IC 7486		0	0	0
			0	1	1
			1	0	1
			1	1	0

Theory:

A logic gate performs a logical operation on one or more logic inputs and produces a single logic output. The logic is normally performed as Boolean logic and is most commonly found in digital circuits.

The different types of logic gates are:

i. NOT gate

ii. OR gate

iii. AND gate

iv. EX-OR gate

v. NAND gate

vi. NOR gate

Inverter or NOT gate:

The inverter is a logic gate which has only one input & one output. In inverter a low input produces a high output and a high input produces a low output.

Logic equation is: $Y = \overline{A}$ Digital IC for NOT: **IC 7404.**

AND gate:

AND gate is a logic gate Which can have two or more inputs. But there is only one output. The output of AND gate is high only if all inputs are high. Even if one input is low, the output will be low.

Logic equation is: **Y = AB** Digital IC for AND: **IC 7408.**

OR gate:

An OR gate is a logic gate Which can have two or more inputs and a single output. The output of an OR gate is high if any of the inputs or all inputs are high. The output is low only if all the inputs are low.

Logic equation is: **Y= A + B** Digital IC for OR: **IC 7432.**

NAND gate:

NAND gate is a combination of AND & NOT gates. Thus NAND gate is
the inverse of AND gate. The output is low when all inputs are high. The output is high for all the remaining combinations.

Logic equation is: $Y = \overline{AB}$ Digital IC for NAND: **IC 7400.**

NOR gate:

NOR gate is a combination of OR & NOT gates. Thus NOR gate is the inverse of OR gate. When all or either of the inputs are high output is low. The output of NOR gate is high only when all inputs are low.

Logic equation is: $Y = \overline{A + B}$ Digital IC for NOR: **IC 7402.**

EX-OR gate:

In EX-OR gate if either of the inputs is high, output will be high. If both the inputs are high output will be low. If both inputs are low then also output will be low.

Logic equation is: $Y = A\overline{B} + B\overline{A} = A \oplus B$ Digital IC for EX-OR: **IC 7486.**

Procedure:

1) Connect 5V adaptor to trainer kit.
2) Make the connection as per symbolic diagram.
3) Connect inputs on data input side and outputs on output sides.
4) Verify given truth tables.

Conclusion:

Thus we have learned on kit design of different logic gates and verification of their truth tables.

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Experiment 6

AIM: To design and implement Arithmetic circuits viz., Half adder and Half substractor.

Apparatus: Logic gate trainer kit, 5V adaptor, connecting wires.

Diagram:

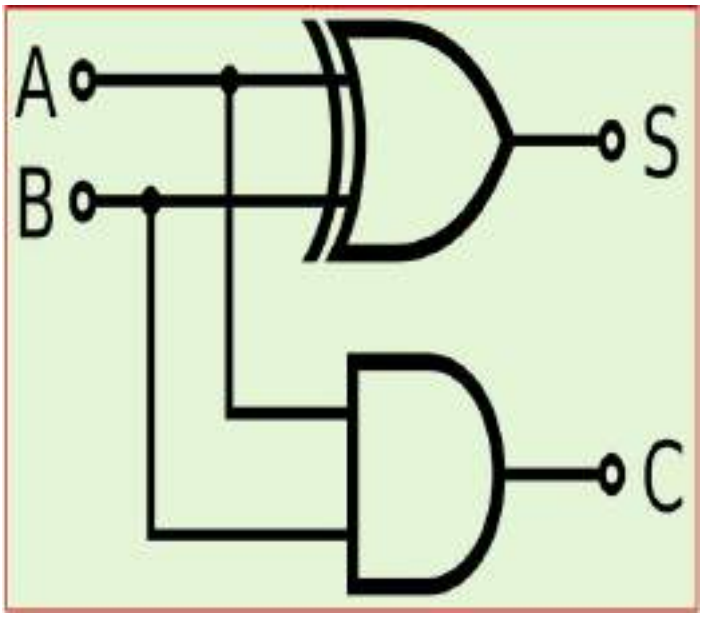


Figure1: Half adder logic diagram

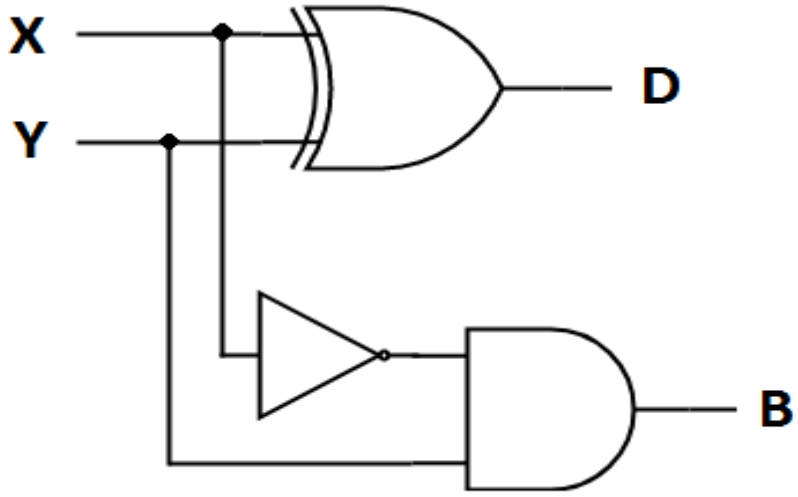


Figure2: Half substractor circuit

Theory: An adder is a digital logic circuit in electronics that implements addition of numbers. In many computers and other types of processors, adders are used to calculate addresses, similar operations and table indices in the ALU and also in other parts of the processors. These can be built for many numerical representations like excess-3 or binary coded

decimal. The half adder circuit has two inputs: A and B, which add two input digits and generate a carry and sum. The full adder circuit has three inputs: A and C, which add the three input numbers and generate a carry and sum.

Half subtractor and full subtractor are basically electronic devices or we can say logical circuits which performs subtraction of two binary digits. We can define half subtractor as a combinational circuit which is capable of performing subtraction of 2-bit binary digits is known as a half subtractor. Here, the binary digit from which the other digit is subtracted is called **minuend** and the binary digit which is to be subtracted is known as the **subtrahend**.

Half Adder Truth Table

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Adder Truth Table

Inputs		Outputs	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Procedure:

1) Connect 5V adaptor to trainer kit.
2) Make the connection as per symbolic diagram.
3) Connect inputs on data input side and outputs on output sides.
4) Verify given truth tables.

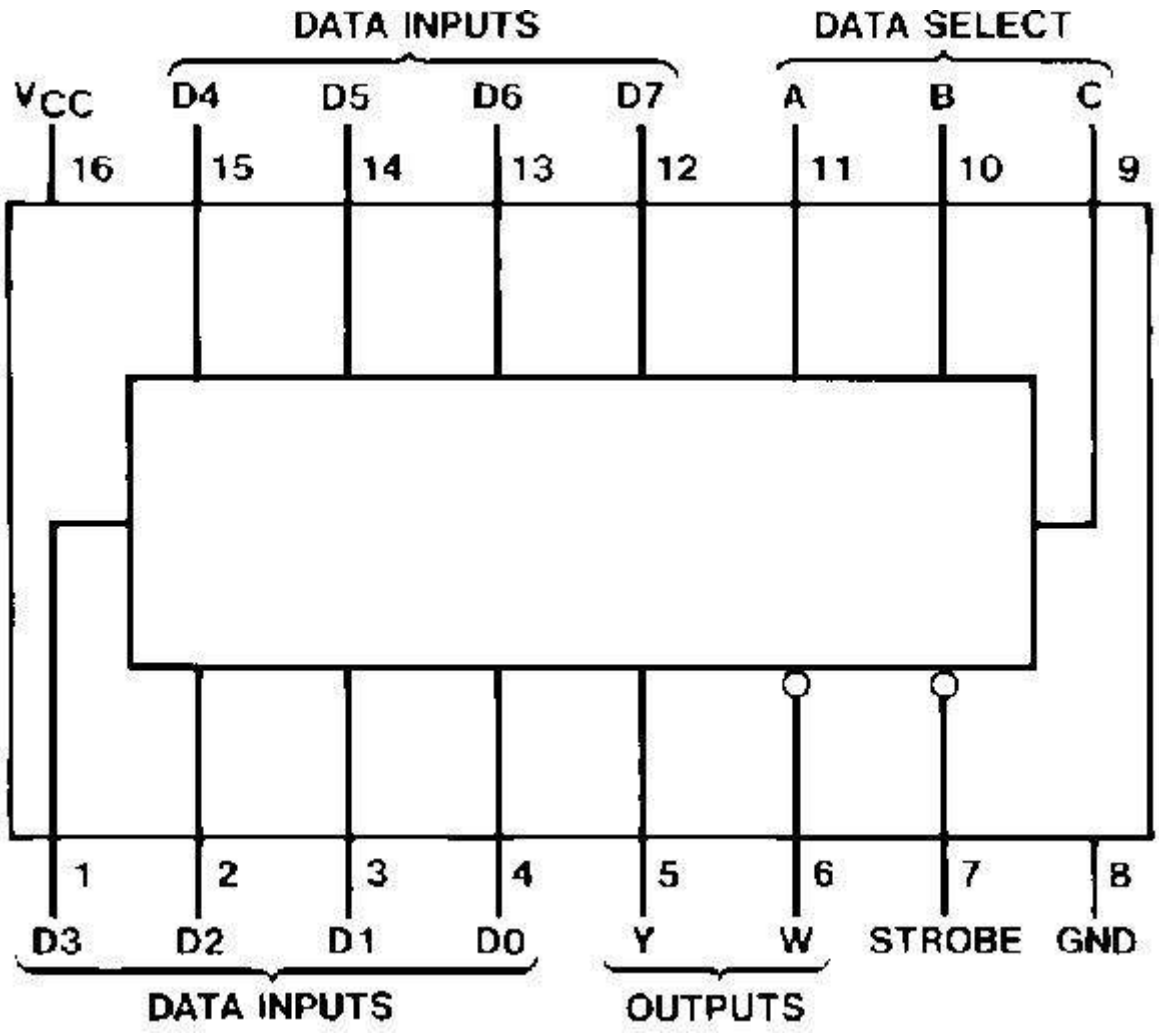
Conclusion:

EXPERIMENT NO 7

AIM: To study 3-STATE 1-of-8 Line Data Selector/Multiplexer

APPARATUS: Bread board, IC 74251, connection wires.

DIAGRAM:



THOERY:

DM74LS251

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled 3-STATE output. The strobe must be at a low logic level to enable these devices. The 3- STATE outputs permit direct connection to a common bus. When the strobe input is HIGH, both outputs are in a high impedance state in which both the upper and lower transistors of each totem-pole output are OFF, and the output neither drives nor loads the bus significantly. When the strobe is LOW, the outputs are activated and operate as standard TTLtotem-pole outputs. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

LOGIC/FUNCTIONAL TABLE:

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

PROCEDURE:

1) Give input voltage as Vpp=12 V to Vcc.
2) Connect pin no 8 to ground.
3) Connect step input enable to pin no.7.
4) Connect respective data inputs.
5) Depending on input the input gate is selected and output is observed same as the input.

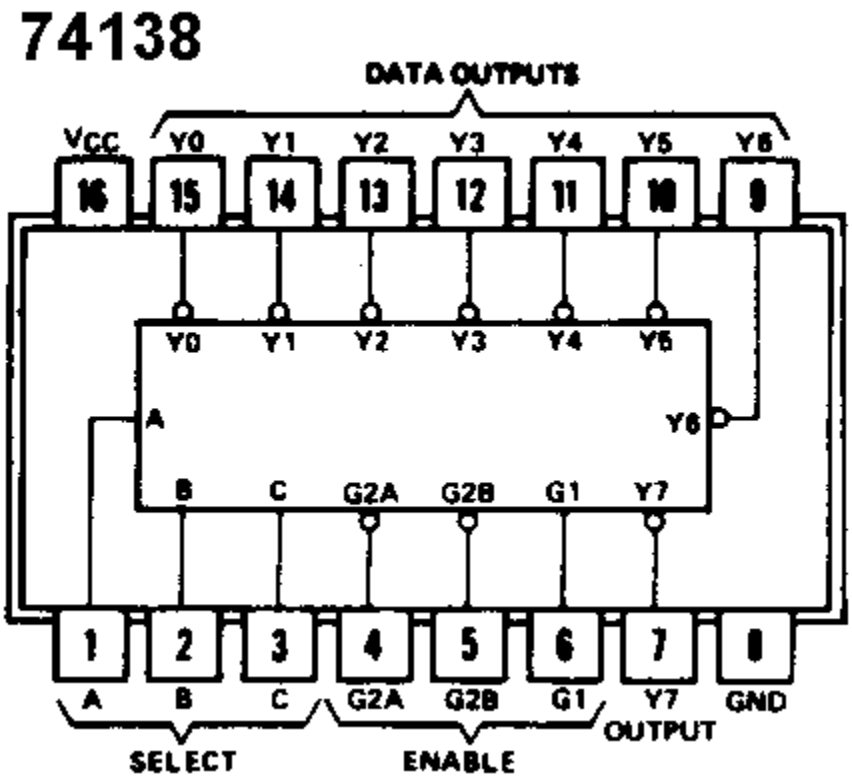
CONCLUSION:
Thus with the help of multiplexer the **INPUT** line gets selected according to select lines.

EXPERIMENT NO 8

AIM: To study 3-STATE 3-of-8 Line Data Selector/ De-multiplexer

APPARATUS: Bread board, IC 74251, connection wires.

DIAGRAM:



FUNCTIONAL TABLE :

Data Input	Select Inputs			Outputs							
D	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

PROCEDURE:

1) Give input voltage as Vpp=12 V to Vcc.
2) Connect pin no 8 to ground.
3) Connect select lines to pin nos.1, 2, 3.
4) Connect respective data outputs to pins 7 and 9 to15.
5) Keep enable input HIGH at pin 6.

CONCLUSION:

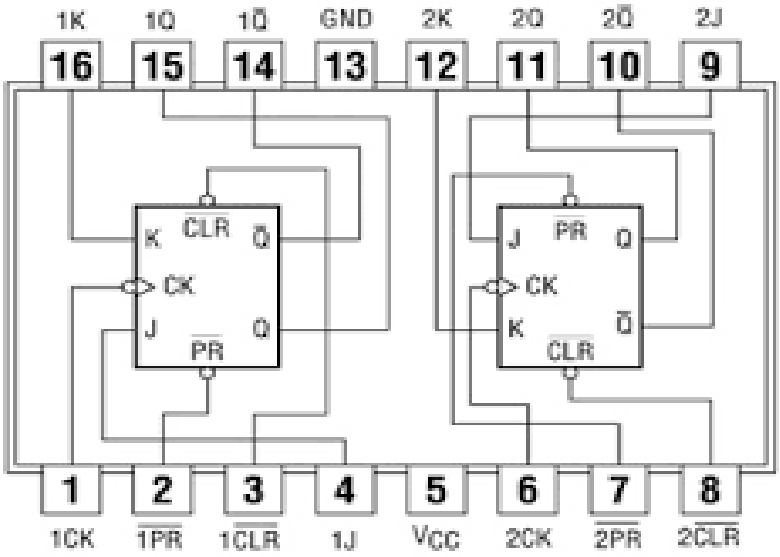
Thus with the help of De-multiplexer the output line gets selected according to select lines.

Experiment No 9

AIM: To Study CLOCK PULSE JK FF.

APPARATUS: Bread board, IC 74251, connection wires.

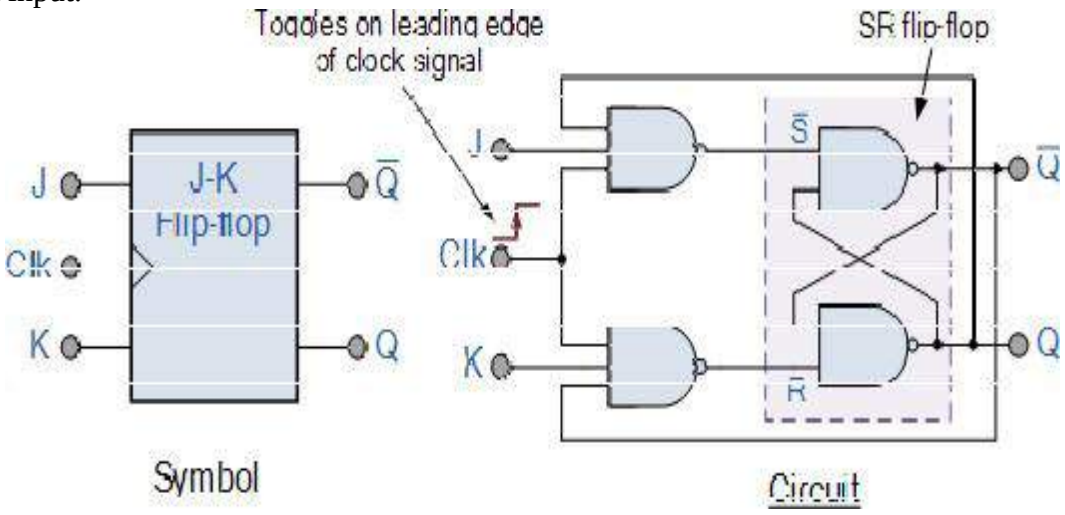
DIAGRAM:



THOERY:

The simple **JK flip-Flop** is the most widely used of all the flip-flop designs and is considered to be a universal flip-flop circuit. The sequential operation of the JK flip-flop is exactly the same as for the previous SR flip-flop with the same "Set" and "Reset" inputs. The difference this time is that the JKflip-flop has no invalid or forbidden input states of the SR Latch (when S and Rare both 1).

The **JK flip-flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1". Due to this additional clocked input, a JK flip-flop has four possible input combinations, "logic 1", "logic 0", "no change" and "toggle". The symbol for a JK flip-flop is similar to that of an **SR Bistable Latch** as seen in the previous tutorial except for the addition of a clock input.



The Basic JK Flip-flop

Both the S and the R inputs of the previous SR bistable have now been replaced by two inputs

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

H = HIGH Logic Level

L = LOW Logic Level

X = Either LOW or HIGH Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is HIGH. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete active HIGH level clock pulse.

Note 1: This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (HIGH) level.

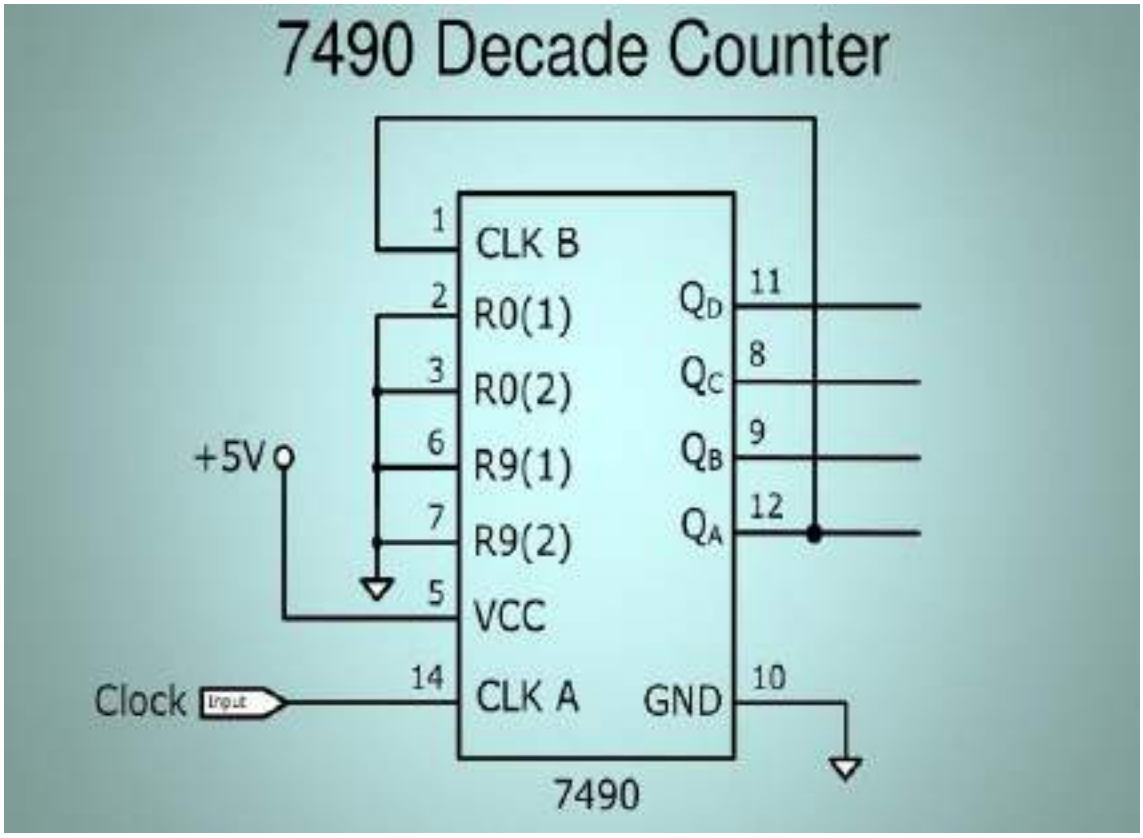
Conclusion: Thus we have studied CLOCK PULSE JK FF and verified truth table of JKFF.

EXPERIMENT 10

AIM : To design and verify MOD 10 counter using IC 7490.

Apparatus: IC 7490, breadboard trainer kit, 5V adaptor, connecting wires.

Diagram:



Theory:

A binary coded decimal (BCD) is a serial digital counter that counts ten digits .And it resets for every new clock input. As it can go through 10 unique combinations of output, it is also called as “Decade counter”. A BCD counter can count 0000, 0001, 0010, 1000, 1001, 1010, 1011, 1110, 1111, 0000, and 0001 and so on.

It is a simple counter which can count from 0 – 9. As it is a 4 bit binary decade counter, it has 4 output ports QA, QB, QC and QD. When the count reaches 10, the binary output is reset to 0 (0000), every time and another pulse starts at pin number 9. The Mod of the IC 7490 is set by changing the RESET pins R1, R2, R3, R4.

If any one of R1 & R2 is at high or R3 & R4 are at ground, the counter will reset all the outputs QA, QB, QC and QD to 0. If the pins R3 & R4 are high, then the count on QA, QB, QC and QD is 1001.

We can increase the counting capability of a Decade number by connecting more ICs n series; we can count 99 with two 7490 ICs connected in series. This 7490 IC has inbuilt Divide by 2 and Divide by 5 counters in it. It can also be used as divide by 10 counter by connecting by connecting clock input 2 and QA and connecting all rest pins to ground and giving pulse input to 1. It is used as divide by 6 counter by supplying pulse at input 1 and grounding reset pins R3 and R4 and connecting QA with input 2.

7490 IC can work like bi –quinary counter, which is used to store decimal digits in the form of 4 bit binary numbers.

Truth Table:

Input Pulses	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
0	0	0	0	0 (resets)

Procedure:

1. Pin 1 is shorted with pin 12.
2. Pins 2,3,6,7 are grounded.
3. Pins 8, 9, 11, 12 are connected on output side.
4. Connect 5V at pin 5 and grounds pin 10.
5. Apply clock pulse at pin 14 and observe the count.

Conclusion:

Thus it is a simple counter which can count from 0 – 9 as per applied clock pulses applied at second input terminal of IC 7490.